REMARKS

This application has been reviewed in light of the Office Action dated September 6, 2007. Claims 1-2 and 4-21 are now pending in the application. Claims 1, 2, 4, 6, 7, 10, 12, 13, 20 and 21 have been amended. Claim 3 has been canceled without prejudice. No new matter has been added. The Examiner's reconsideration of the rejection in view of the following remarks is respectfully requested.

By the Office Action, FIG. 6 was objected to stating that the rectangular boxes were not labeled. While it is respectfully submitted that FIG. 6 represents a hardware configuration and is properly labeled, an amended drawing sheet is submitted herewith to further prosecution of the case. Reconsideration is respectfully requested.

By the Office Action, claims 1-13, 15-18 and 20-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Japanese Publication, JP 2001-30511, hereinafter Murai in view of U.S. Publication No. 2002/0084967, hereinafter Akimoto.

Murai is directed to a pixel circuit having transistors 13 and 14 having a common input. The output of these transistors is connected to an additional transistor 15. As the Examiner has stated, Murai does not teach a capacitive connection between the gate and the output of one of the switching transistors. Akimoto was cited to cure this deficiency.

In Akimoto, the Examiner points to FIG. 23 and in particular transistor 87 with a capacitor 88 to teach a capacitive connection. However, the circuit includes diodes 89 and 91 and capacitor 90 coupled to the output of transistor 87. Further a second transistor 93 has its output connected to ground 36 via a separate capacitor 5. Transistor 87 is employed as a rewrite switch, which is used to refresh the pixel without reusing the signal line (see FIG. 23 and the

accompanying text). The rewrite transistor is employed for a completely different purpose from the present claims.

Claim 1 recites, *inter alia*, a device comprising ... at least first and second switching transistors connected between a respective one of the at least two inputs and the pixel element,... and wherein a capacitive connection is provided between the gate of at least one of the switching transistors and a **common output node** of the switching transistors.

The present principles teach first and second switching transistors connected at their gates along with a capacitive connection also connected to their gates and to a common output node of the transistors. In this way, the capacitance is shared between the transistors such that a single data signal can be applied to both transistors to simultaneously switch one transistor on and the other off.

Akimoto fails to disclose or suggest at least: a capacitive connection provided between the gate of at least one of the switching transistors and a common output node of the switching transistors as provided in amended claim 1. Akimoto not only fails to disclose or suggest the structure of claim 1, but also fails to teach or suggest the problem or the solution addressed in accordance with the present invention. The rewrite switch (transistor) 87 of Akimoto includes a bootstrapped capacitor to store energy to preserve the pixel signal, and not to provide a single data signal that can be applied to two switching transistors to simultaneously switch one transistor on and the other off. This improves performance by, e.g., at least reducing a voltage swing needed between on and off voltage levels of a data signal, among other things.

Therefore, Murai and/or Akimoto, taken singly or in combination, fail to disclose or suggest at least: a capacitive connection provided between the gate of at least one of the switching transistors and a common output node of the switching transistors as recited in claim 1

and as essentially recited in claim 20. The cited combination fails to disclose or suggest all of the elements in claim 1 and claim 20, and, in addition, fails to address the problems of the present disclosure. Claims 1 and 20 are therefore believed to be in condition for allowance for at least the stated reasons. Further, dependent claims 2, 4-6, 12-19 and 21 are also believed to be in condition for allowance due at least to their dependency from claims 1 and 20, respectively.

Claim 10 has been amended to include the subject matter of previously presented claims 1 and 6. Claim 10 recites, *inter alia*, ... a capacitive connection comprises a respective capacitor connected between the gate of each switching transistor and an output of the switching circuit, the device further comprising n inputs, and comprising first to nth switching transistors connected between a respective one of the n inputs and one of two intermediate outputs, and wherein the data signals for each switching transistor are selected such that half of the switching transistors are turned on to route a first selected input to one intermediate output and to route a second selected input to the other intermediate output.

It is respectfully submitted that the combination of Murai and Akimoto also fails to teach or suggest at least that a capacitive connection comprises a respective capacitor connected between the gate of each switching transistor and an output of the switching circuit, the device further comprising n inputs, and comprising first to nth switching transistors connected between a respective one of the n inputs and one of two intermediate outputs, and wherein the data signals for each switching transistor are selected such that half of the switching transistors are turned on to route a first selected input to one intermediate output and to route a second selected input to the other intermediate output. The Examiner stated that items 61 and 62 of Murai teach the intermediate outputs. Item 61 is a transistor in FIG. 6 of Murai but does not teach or suggest an

intermediate output as recited in claim 10. Further, item 62 was not found in the FIGS. of Murai. In fact, no similar structure has been found in either Murai or Akimoto.

Therefore, claim 10 is believed to be in condition for allowance over the cited combination for at least the reasons stated. Dependent claims 7-9 and 11 are also believed to be in condition for allowance due at least to their dependency from claim 10. Reconsideration of the rejection is earnestly solicited.

By the Office Action, claim 14 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Murai in view of Akimoto and further in view of PCT Publication No. WO 01/40857 (U.S. Publication No. 2002/0158993, hereinafter Murai '993), and claim 19 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Murai in view of Akimoto and further in view of U.S. Patent No. 5,105,288, hereinafter Senda).

While the Applicant respectfully disagrees with these rejections, claims 14 and 19 depend from claim 1 and are believed to be in condition for allowance at least due to this reason. Reconsideration of the rejection is earnestly solicited.

In view of the foregoing amendments and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to applicant's representatives Deposit Account No. 14-1270.

Respectfully submitted,

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